Course Code: 20EC0411 **R20**

SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY :: PUTTUR

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QUESTION BANK (DESCRIPTIVE)

Subject with Code: LDICA (20EC0411) **Course & Branch**: B.Tech – ECE

Year &Sem: II-B.Tech & II-Sem **Regulation:** R20

UNIT –I
OP AMP CHARACTERISTICS AND LINEAR APPLICATIONS

1	**a)**	Define Integrated Circuit.	[L1] [CO1]	**[2M]**
	b)	Draw the Op-Amp Symbol & Mention the terminals.	[L1] [CO1]	**[2M]**
	c)	Define Virtual Ground Property.	[L1] [CO1]	**]2M]**
	d)	Compare and contrast the ideal and practical Op-Amp of IC 741.	[L2] [CO1]	**[6M]**
2	**a)**	Determine the output voltage of a differential Amplifier for the input voltages of 300µV & 240µV.The Differential gain of the amplifier is 5000.the value of the CMRR is 100.	[L3] [CO1]	**[6M]**
	b)	Draw the block diagram of Op-Amp and explain each block.	[L1] [CO2]	**[6M]**
3	**a)**	Explain any two DC characteristics of Op-Amp with relevant expressions.	[L2] [CO3]	**[6M]**
	b)	Discuss about AC characteristics of an Op-Amp with relevant expressions.	[L2] [CO3]	**[4M]**
	c)	List the features of Op-Amp.	[L1] [CO1]	**[2M]**
4	**a)**	Derive the output voltage for Inverting adder.	[L3] [CO4]	**[6M]**
	b)	Derive the output voltage for non-Inverting adder	[L3] **[**CO4]	**[6M]**
5	**a)**	How an Op-amp acts as a Differential amplifier? Justify.	[L2] [CO4]	**[8M]**
	b)	Write the Applications of an Op-Amp.	[L1] [CO4]	**[4M]**
6	**a)**	With neat sketch explain the operation of an Instrumentation amplifier.	[L3] [CO4]	**[8M]**
	b)	Explain the operation of an Inverting A.C Amplifier.	[L2] [CO4]	**[4M]**
7	**a)**	Explain about the Non-Inverting A.C Amplifier.	[L2] [CO4]	**[4M]**
	b)	Draw the circuit and explain the working of Voltage to current converter.	[L1] [CO1]	**[8M]**
8	**a)**	Draw the circuit and explain the working of Current to voltage converter.	[L1] [CO4]	**[6M]**
	b)	Explain about the operation of sample and hold circuit with relevant Waveforms and neat sketch.	[L2] [CO4]	**[6M]**
9		Derive the output expressions of the following.	[L3] [CO4]	
	a)	Differentiator.		**[6M]**
	b)	Integrator.		**[6M]**
10		Explain the followings with neat sketch.	[L2] [CO4]	
	a)	Inverting comparator.		**[4M]**
	b)	Non-Inverting comparator.		**[4M]**
	c)	Discuss about Schmitt trigger with neat circuit diagram and waveforms.	[L2] [CO4]	**[4M]**

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UNIT –II
ACTIVE FILTERS, OSCILLATORS & TIMERS

1	**a)**	Define Filter.	[L1] [CO1]	**[2M]**
	b)	Draw the circuit of a 1st order low pass Butterworth filter and discuss its transfer function.	[L1] [CO4]	**[10M]**
2	**a)**	List the types of Filters.	[L1] [CO1]	**[2M]**
	b)	Derive the gain of a 1st order high pass Butterworth filter	[L3] [CO4]	**[10M]**
3	**a)**	Compare the low pass and high pass filters.	[L4] [CO1]	**[6M]**
	b)	Sketch the frequency response of narrow band pass filter for various input frequencies.	[L3] [CO4]	**[6M]**
4	**a)**	Explain wide band pass filter with neat circuit diagram.	[L2] [CO4]	**[6M]**
	b)	Illustrate the operation of wide Band-Reject Filter.	[L3] [CO4]	**[6M]**
5	**a)**	Differentiate Band pass and Band-Reject Filter.	[L4] [CO4]	**[6M]**
	b)	Why All pass filter is called delay equalizer with neat diagram explain it.	[L4] [CO4]	**[6M]**
6	**a)**	Define Oscillator. List the types of oscillators	[L1] [CO1]	**[4M]**
	b)	Derive the frequency of RC phase shift oscillator using Op-Amp	[L3] [CO4]	**[8M]**
7	**a)**	Derive the frequency of Wein Bridge Oscillator using Op-Amp	[L3] [CO4]	**[8M]**
	b)	Discuss the pin diagram of 555 timer.	[L2] [CO2]	**[4M]**
8	**a)**	Explain the functional block diagram of 555 timer.	[L2] [CO2]	**[10M]**
	b)	Discuss about the Discharge and control voltage pin role in the 555 timer.	[L2] [CO2]	**[2M]**
9	**a)**	With the help of schematic diagram explain how 555 timer can be used as Monostable multivibrator.	[L4] [CO4]	**[6M]**
	b)	Explain the operation of Astable multivibrator using 555 timer and also derive the expression for frequency of oscillation.	[L2] [CO4]	**[6M]**
10	**a)**	Draw the free running oscillator using 555 timer and also derive the expression for frequency of oscillation.	[L3] [CO2]	**[8M]**
	b)	List out any four application of multivibrator.	[L1] [CO1]	**[4M]**

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UNIT –III
PHASE LOCKED LOOPS, CONVERTERS & CMOS LOGIC

1	**a)**	Draw and Explain about the block schematics of PLL.	[L2][CO2]	**[8M]**
	b)	Define PLL and List the applications of PLL.	[L1][CO1]	**[4M]**
2	**a)**	Draw and Explain the block diagram of Monolithic IC 565.	[L2][CO2]	**[6M]**
	b)	Explain the basic structure of DAC.	[L2][CO2]	**[6M]**
3	**a)**	Draw and explain the weighted resistor DAC.	[L2][CO4]	**[6M]**
	b)	Draw and explain the operation of R-2R DAC.	[L2][CO4]	**[6M]**
	a)	List the types of ADC.	[L1][CO1]	**[2M]**
4	**b)**	Explain about parallel comparator ADC with neat block diagram.	[L2][CO4]	**[10M]**
5		Explain about counter type ADC with neat block diagram.	[L2][CO4]	**[12M]**
6	**a)**	The basic step of a 9-bit DAC is 10.3 mV. If "000000000" represents 0V. What output is produced if the input is "101101111"?	[L1][CO3]	**[3M]**
	b)	Explain about flash type ADC.	[L2][CO4]	**[9M]**
7		Draw and explain successive approximation type ADC with an Example.	[L2][CO4]	**[12M]**
8	**a)**	Draw the circuit diagram of Dual Slope ADC and explain its working with neat sketch.	[L2][CO4]	**[9M]**
	b)	Write any three specifications of DAC/ADC?	[L1][CO1]	**[3M]**
9	**a)**	Draw the circuit diagram of basic CMOS gate and explain its operation.	[L2][CO5]	**[4M]**
	b)	Explain the bi-polar logic family.	[L2][CO5]	**[4M]**
	c)	Explain about different logic gates using transistor Logic.	[L3][CO5]	**[4M]**
10	**a)**	Discuss about low voltage CMOS and Interfacing.	[L2][CO5]	**[6M]**
	b)	Explain in detail about basic ECL logic circuit.	[L2][CO5]	**[6M]**

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UNIT –IV
HARDWARE DESCRIPTION LANGUAGES

1	**a)**	Explain the HDL Digital design flow.	[L2][CO5]	**[6M]**
	b)	Explain about VHDL program structure.	[L2][CO5]	**[6M]**
2	**a)**	Explain the various data types supported by VHDL. Give the necessary examples.	[L2][CO5]	**[6M]**
	b)	Discuss about constants and arrays with an example?	[L2][CO6]	**[6M]**
3	**a)**	Write the syntax for functions and procedures with an example?	[L1][CO6]	**[6M]**
	b)	Explain about libraries and packages.	[L2][CO5]	**[6M]**
4	**a)**	Write about structural design elements with an example.	[L3][CO6]	**[12M]**
	b)	Design the logic circuit and write a VHDL program for the following function. F (P) = ΣA, B, C, D (1,5,6,7,9,13) + d (4,15) using structural model.	[L4][CO6]	**[6M]**
5	**a)**	Write about data flow design elements with an example.	[L3][CO6]	**[6M]**
	b)	Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c+d) Also draw the relevant logic diagram.	[L4][CO6]	**[6M]**
6		Design the logic circuit and write VHDL program for the following function. F(X) = Σ A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11).	[L4][CO6]	**[12M]**
7		Design the logic circuit and write VHDL program for the following function. F(Y) = Π A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).	[L4][CO6]	**[12M]**
8		Design the logic circuit and write VHDL program for the following function. F(Y) = **Σ** A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).	[L4][CO6]	**[12M]**
9		Explain in detail different modeling styles of VHDL with suitable examples.	[L2][CO6]	**[12M]**
10	**a)**	Explain the behavioral design elements of VHDL.	[L2][CO5]	**[6M]**
	b)	What is the importance of time dimension in VHDL and explain.	[L2][CO5]	**[6M]**

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UNIT –V

COMBINATIONAL & SEQUENTIAL LOGIC DESIGN PRACTICES

1	**a)**	Design a 4 to 16 decoder with 74×138 IC's.	[L3][CO6]	**[6M]**
	b)	Write a VHDL program for the above design.	[L4][CO6]	**[6M]**
2	**a)**	Explain the operation of standard IC for 3X8 decoder with necessary truth table and internal architecture.	[L2][CO6]	**[6M]**
	b)	Write a VHDL code for the above Decoder	[L1][CO6]	**[6M]**
3		Design a priority encoder that can handle 32 requests. Use 74×148 and required discrete gates. Provide the truth table and explain the operation.	[L3][CO6]	**[12M]**
4	**a)**	Draw the logic symbol of 74 x 85, 4-bit comparator and write a VHDL code for it.	[L1][CO6]	**[6M]**
	b)	Design a 16-bit comparator using 74×85 ICs	[L3][CO5]	**[6M]**
5	**a)**	With the help of logic diagram explain 74×157 multiplexer.	[L4][CO6]	**[6M]**
	b)	Write a VHDL code for the above IC in data flow style.	[L4][CO5]	**[6M]**
6	**a)**	Design a Full adder with Half adder's logic circuit.	[L3][CO6]	**[6M]**
	b)	Write VHDL code for the above design in structural model.	[L4][CO5]	**[6M]**
7	**a)**	Distinguish between latch and flip flop. Show the logic diagram for both. Explain the operation with the help of function table.	[L4][CO6]	**[6M]**
	b)	Write a VHDL code for a D-flip flop in behavioral model.	[L4][CO5]	**[6M]**
8	**a)**	Design a synchronous 4-bit up counter.	[L3][CO6]	**[6M]**
	b)	Write a VHDL code for the above design.	[L4][CO5]	**[6M]**
9	**a)**	Distinguish between the synchronous and asynchronous counters.	[L4][CO6]	**[6M]**
	b)	Design an 8-bit serial in and parallel out shift register.	[L3][CO6]	**[6M]**
10		Design an 8 -bit serial in and serial out shift register and write a VHDL code for it.	[L3][CO6]	**[12M]**